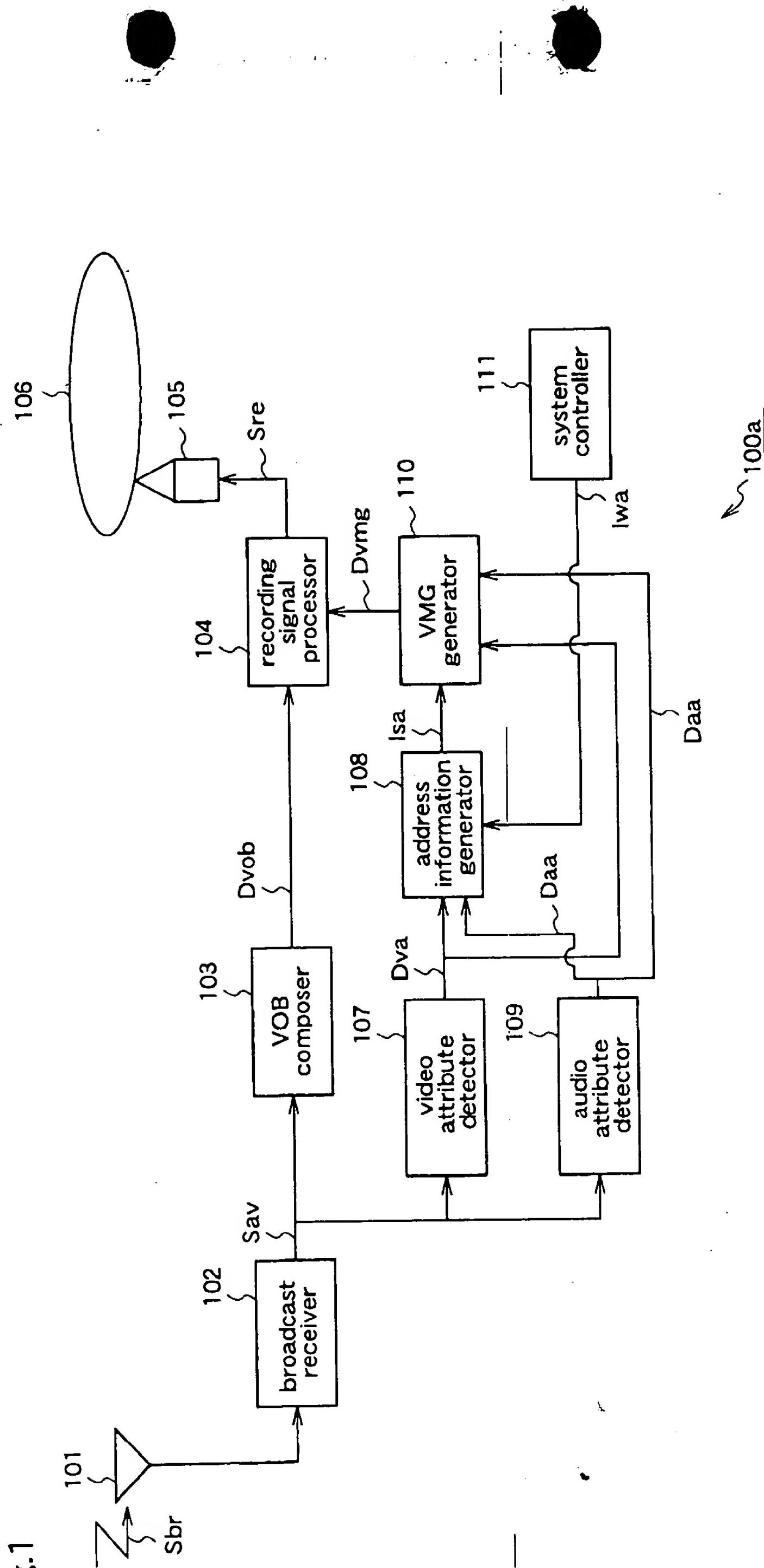


101 Sbr  
102 broadcast receiver  
103 VOB composer  
104 recording signal processor  
105 Sre  
106  
107 video attribute detector  
108 address information generator  
109 audio attribute detector  
110 VMG generator  
111 system controller  
100a

Fig. 1



**Fig.2**

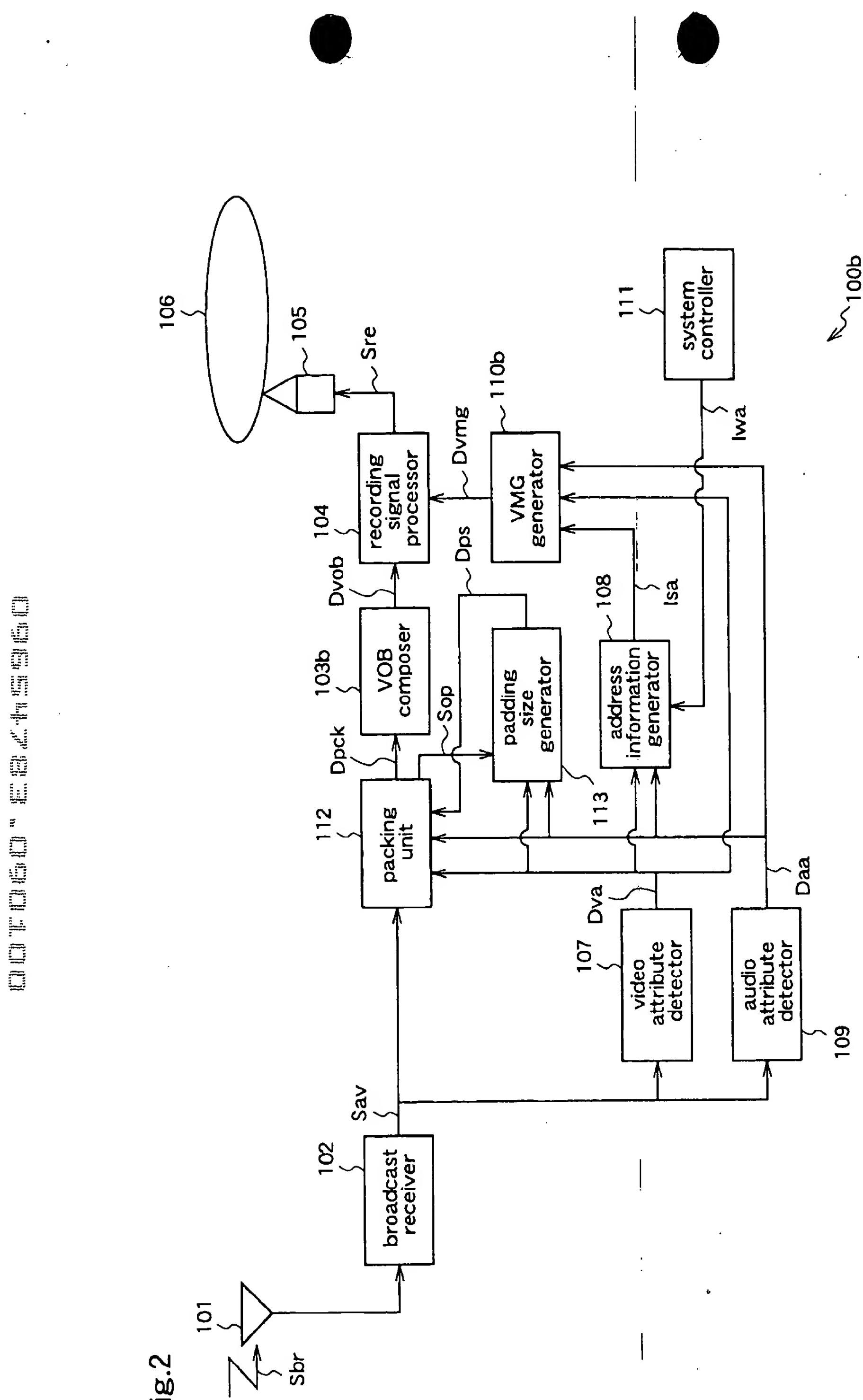
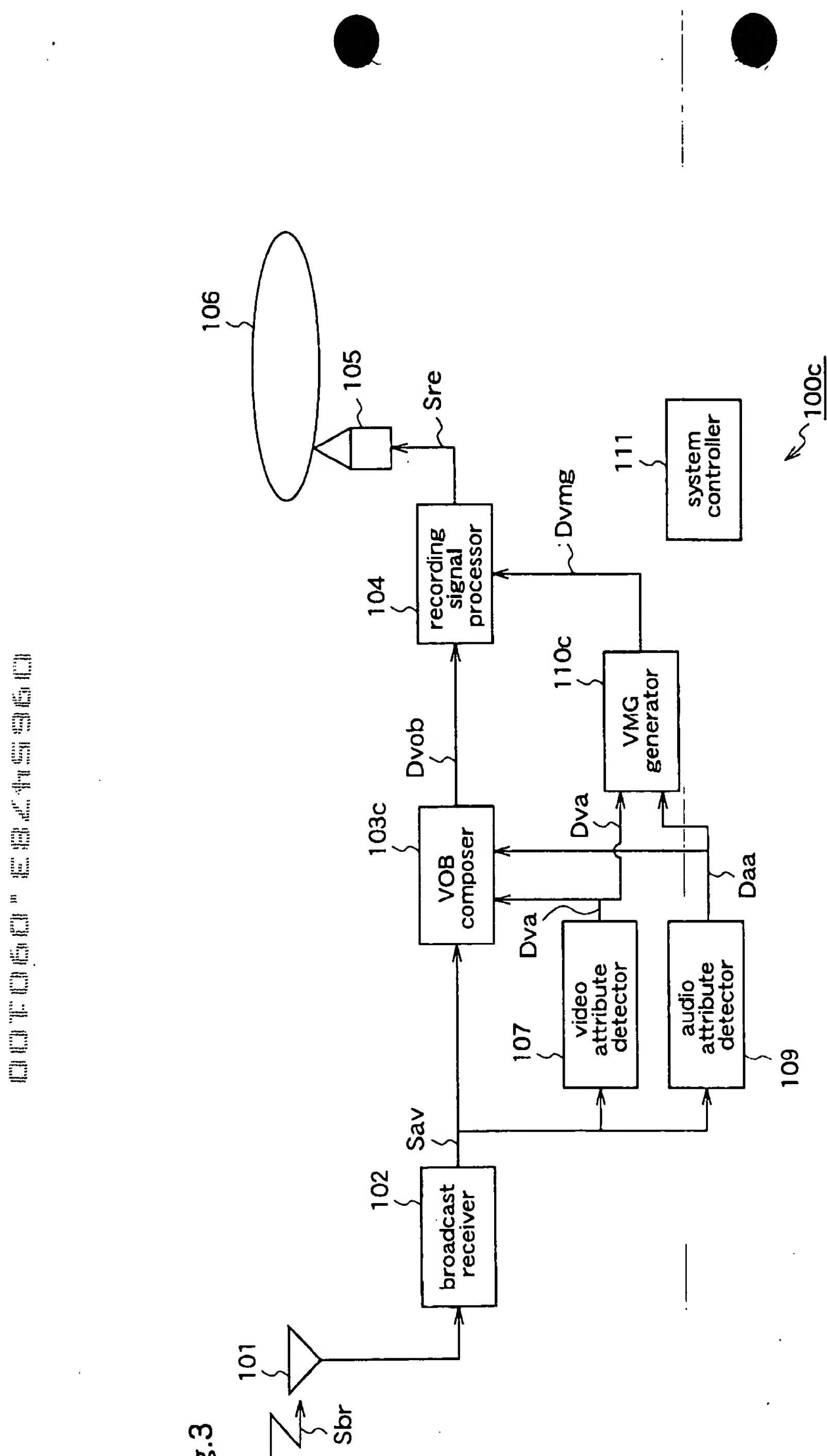


Fig. 3



□ □ □ □ □ □ □ □ □ □ □ □ □

Fig.4

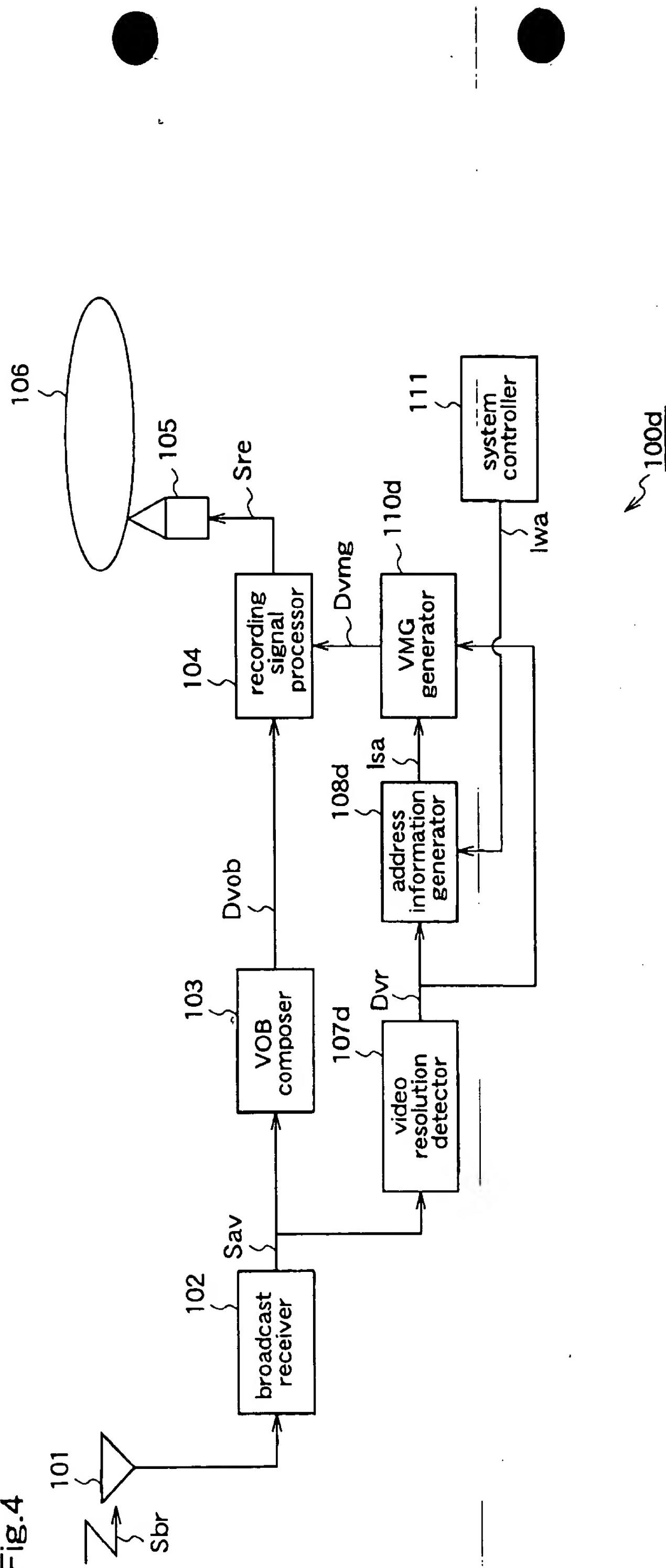
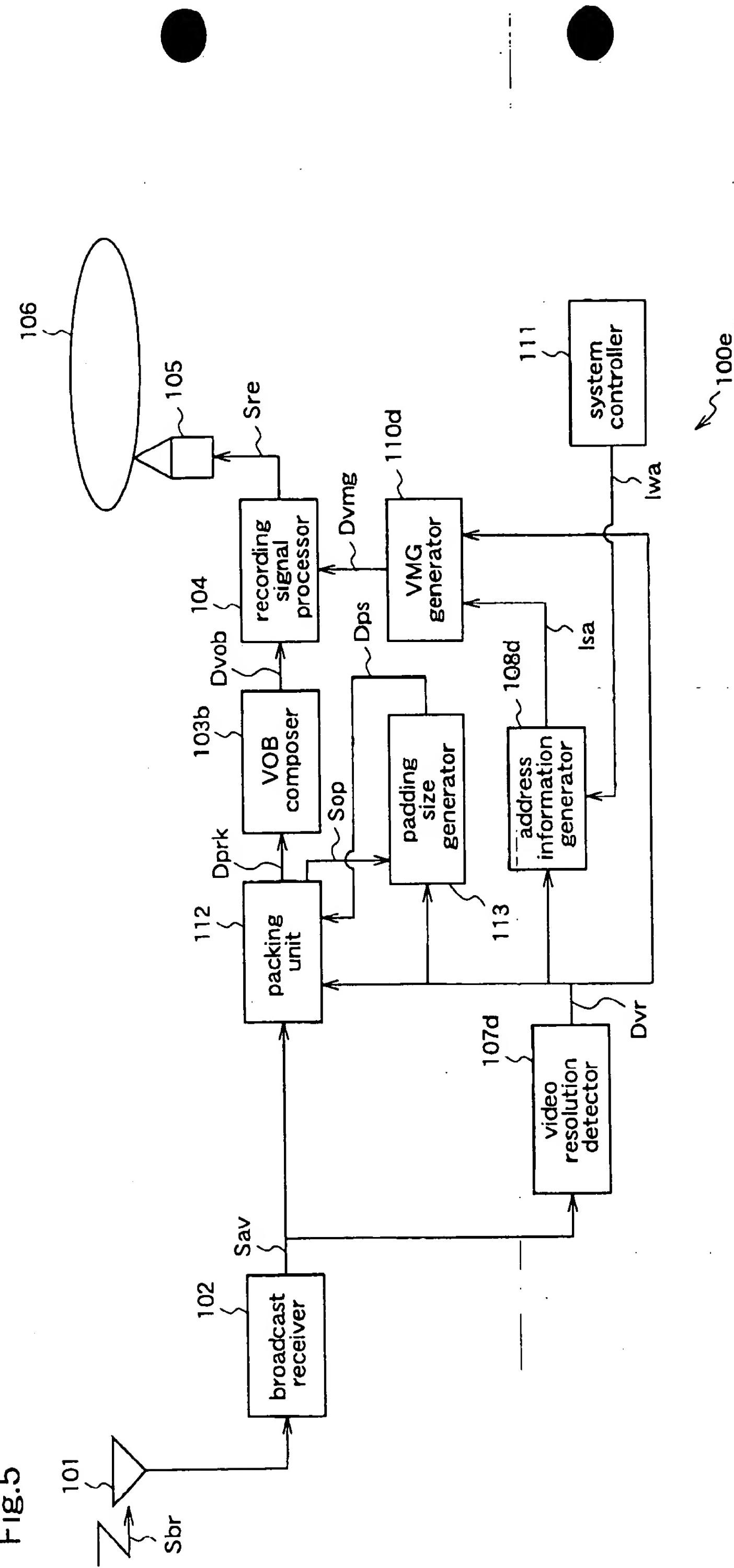


FIGURE 5 - FIGURE 5

Fig.5



100f

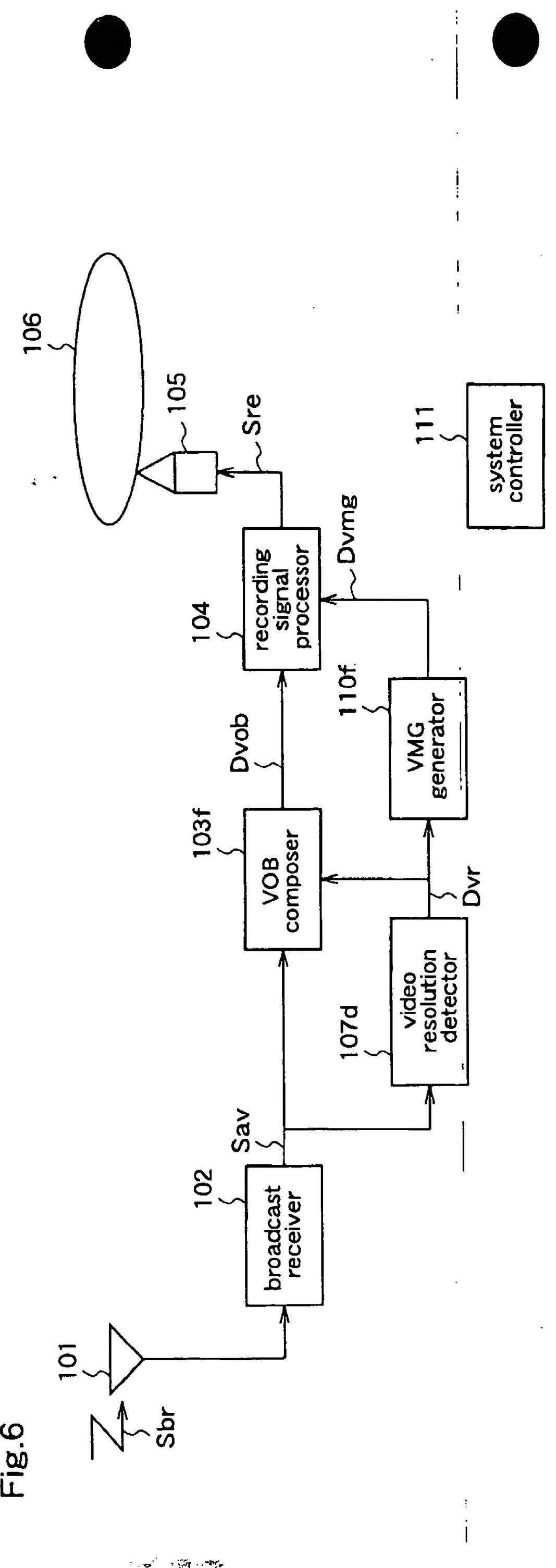
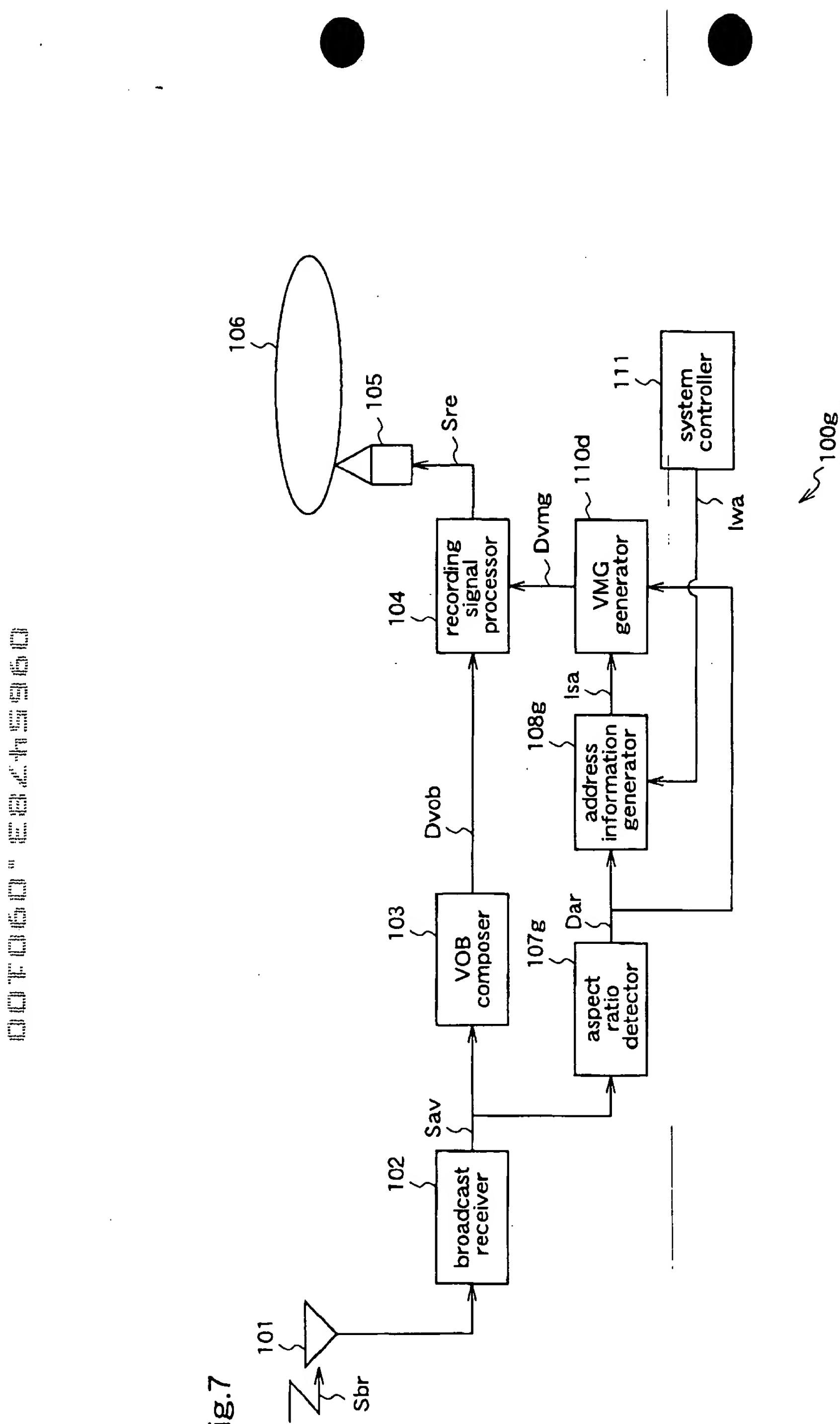


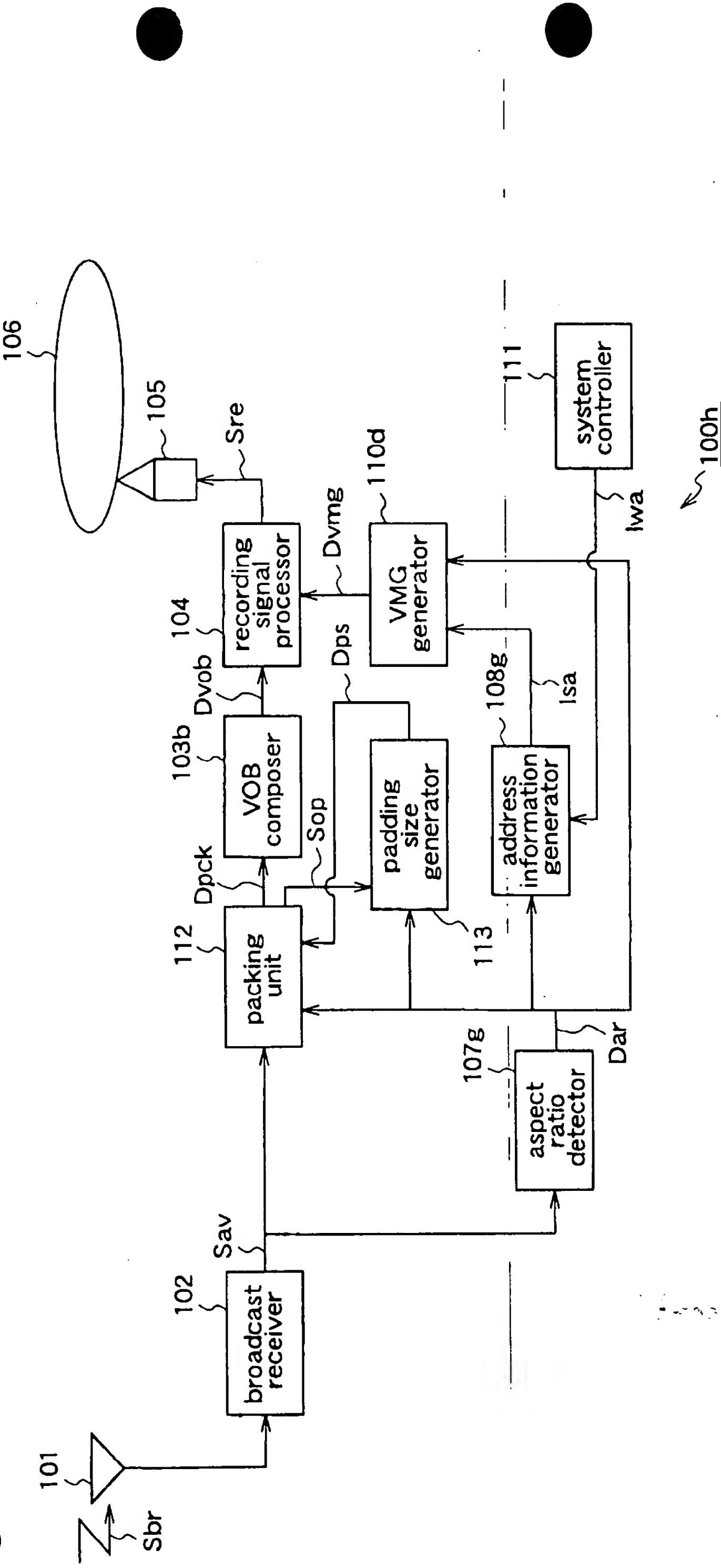
Fig.6

Fig.7



[C] [D] [E] [F] [G] " [E] [D] " [H] [G] [I] [J]

Fig.8



၈၁

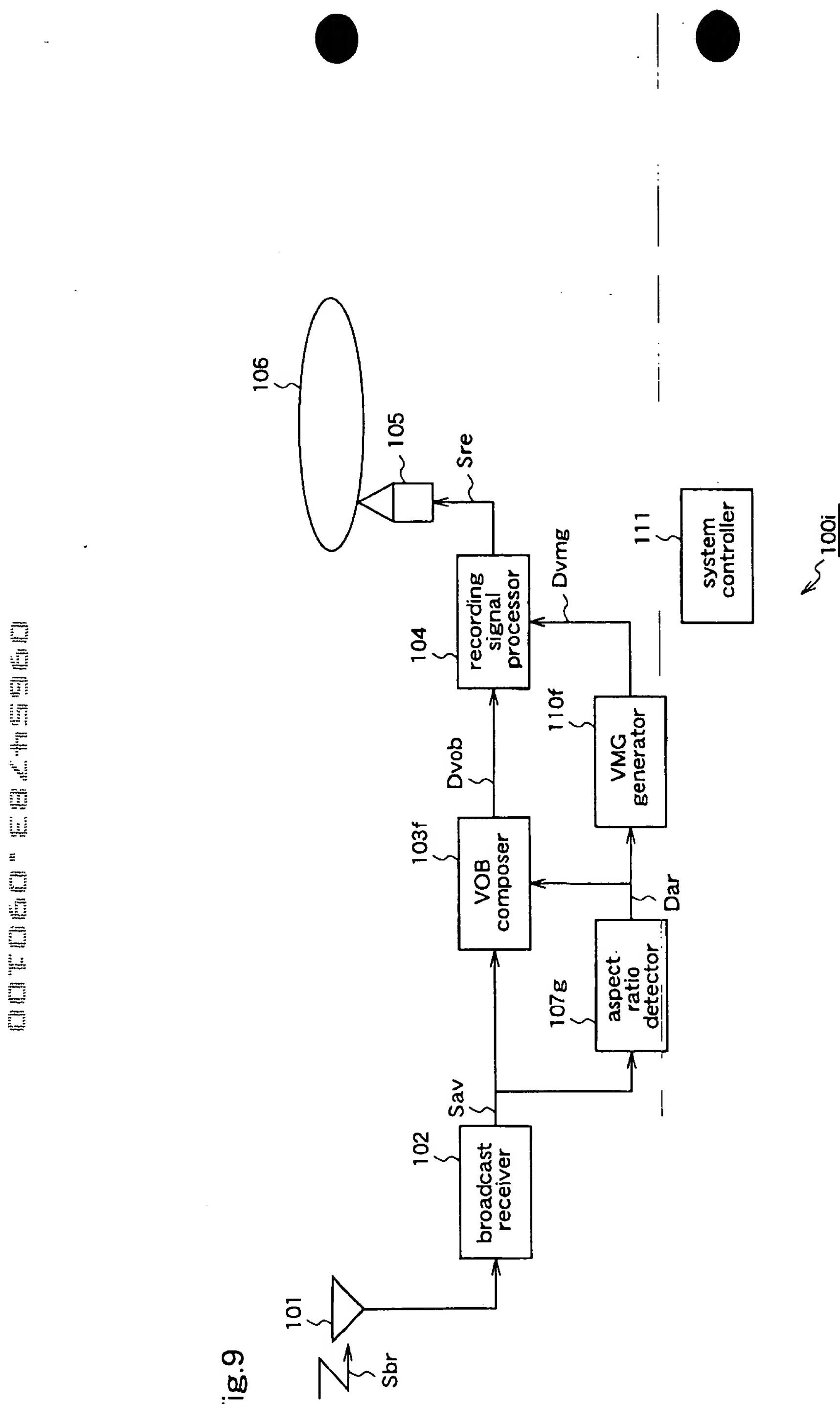
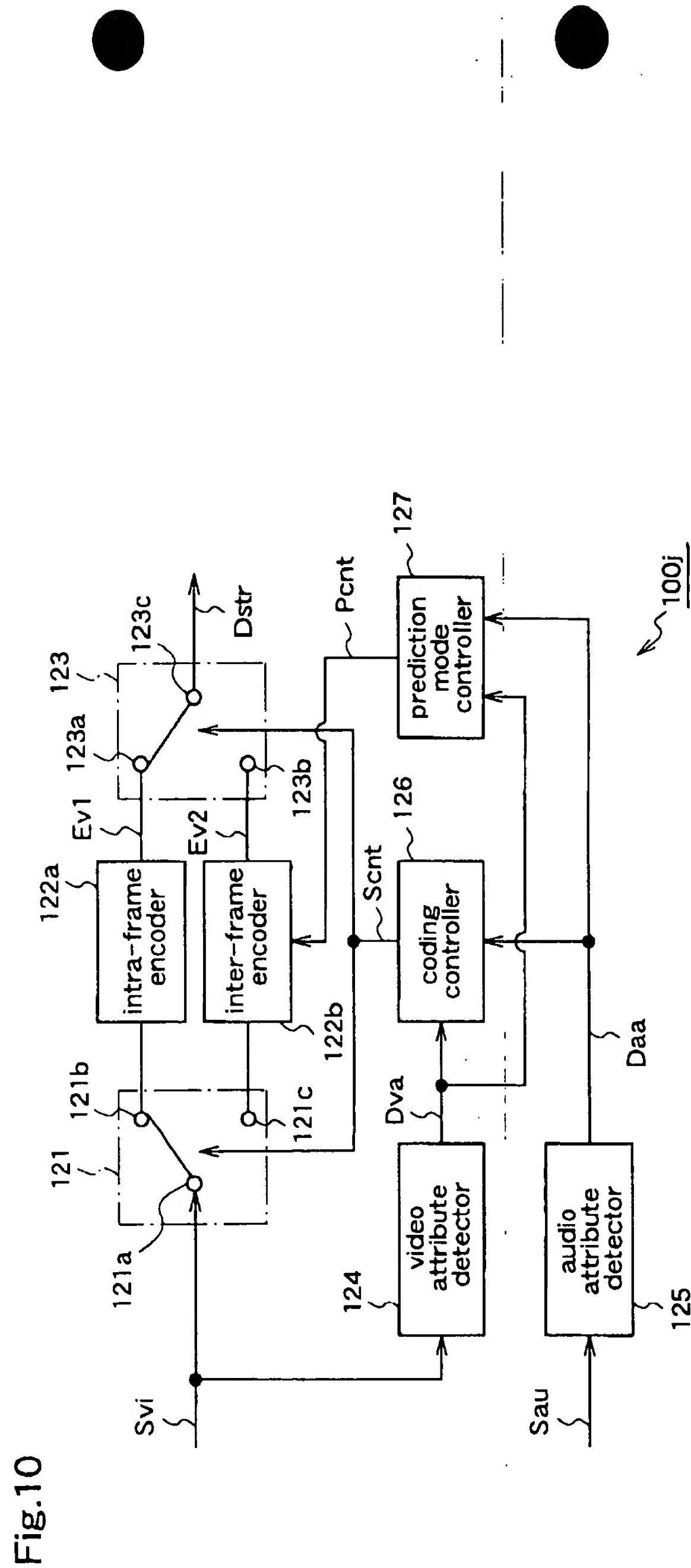
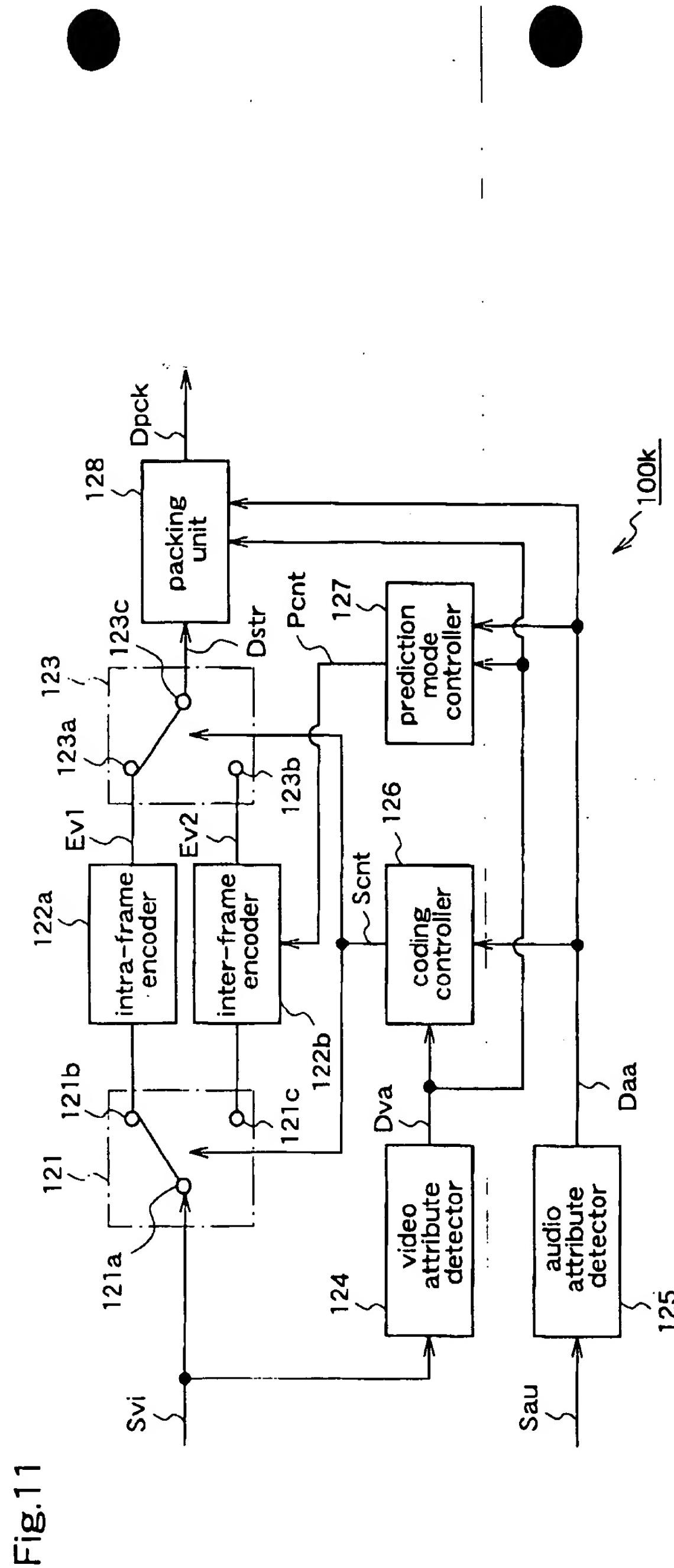


Fig. 10

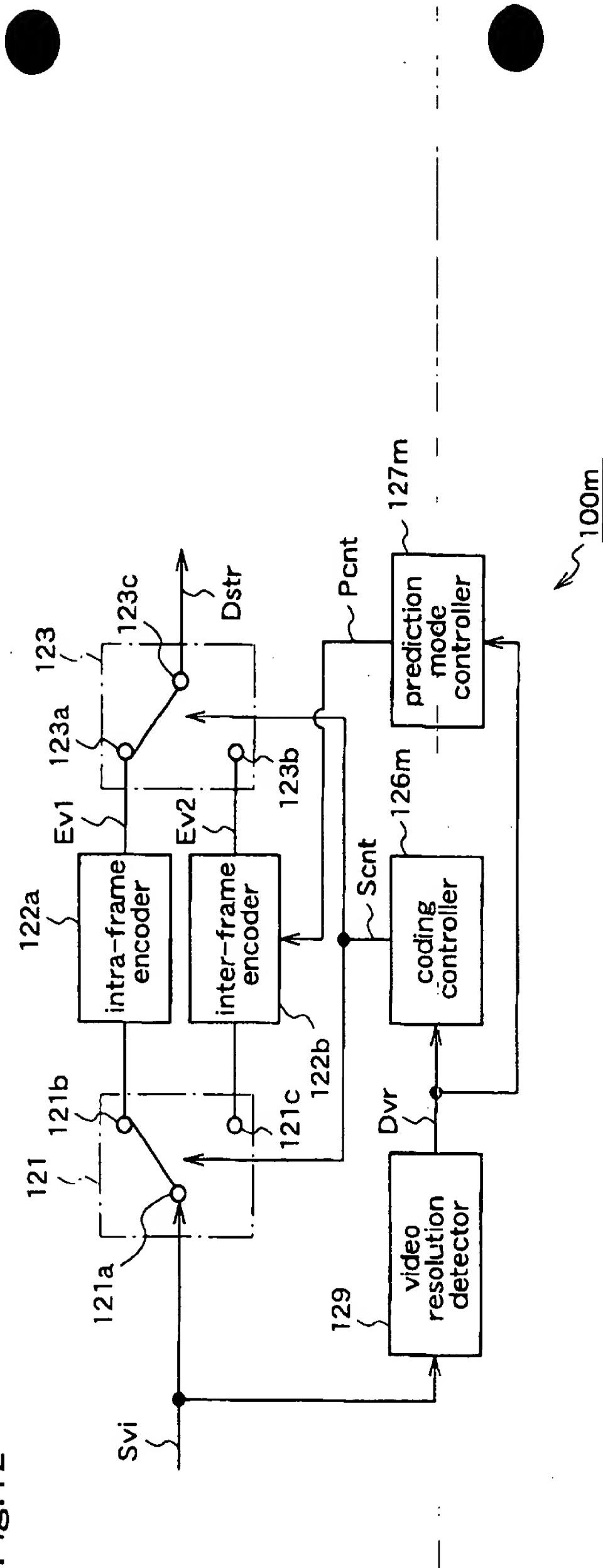


121 121a 121b 121c 122a 122b 122c 123a 123b 123c 124 125 126 127 128



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Fig. 12



**Fig. 13**

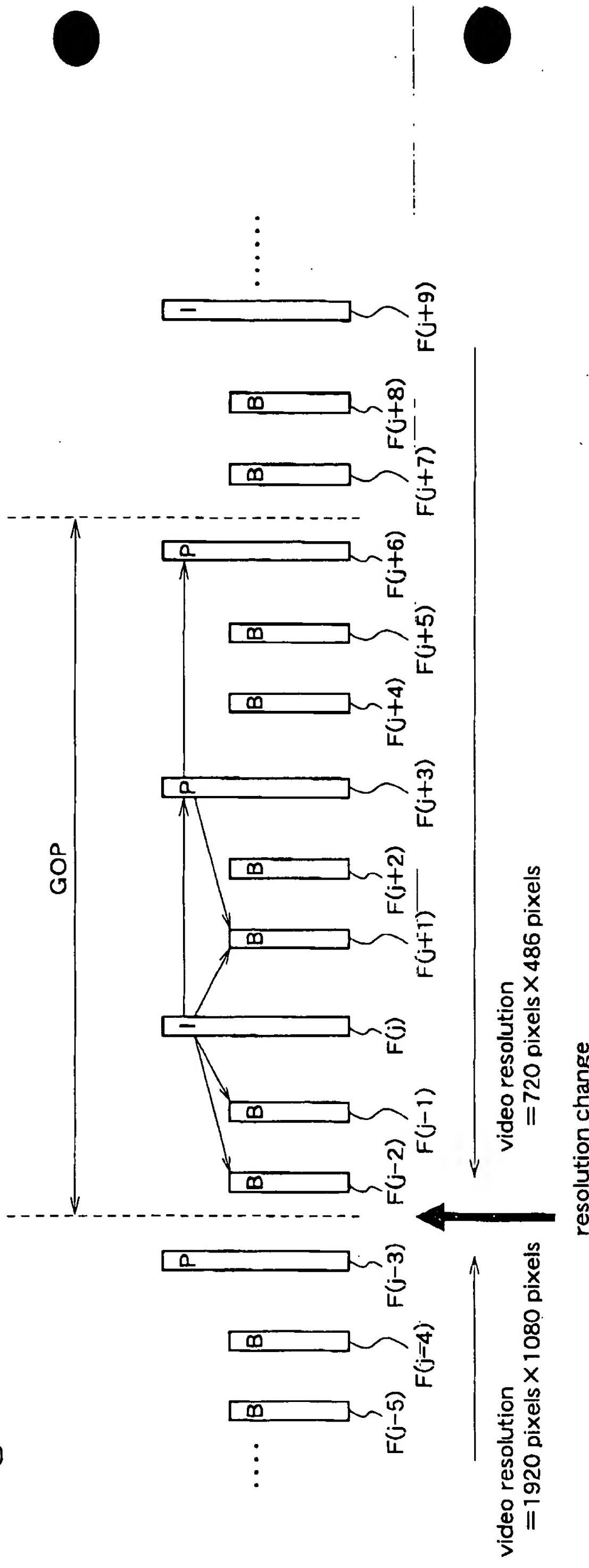


Fig. 14. Block diagram of a video compression system.

Fig. 14

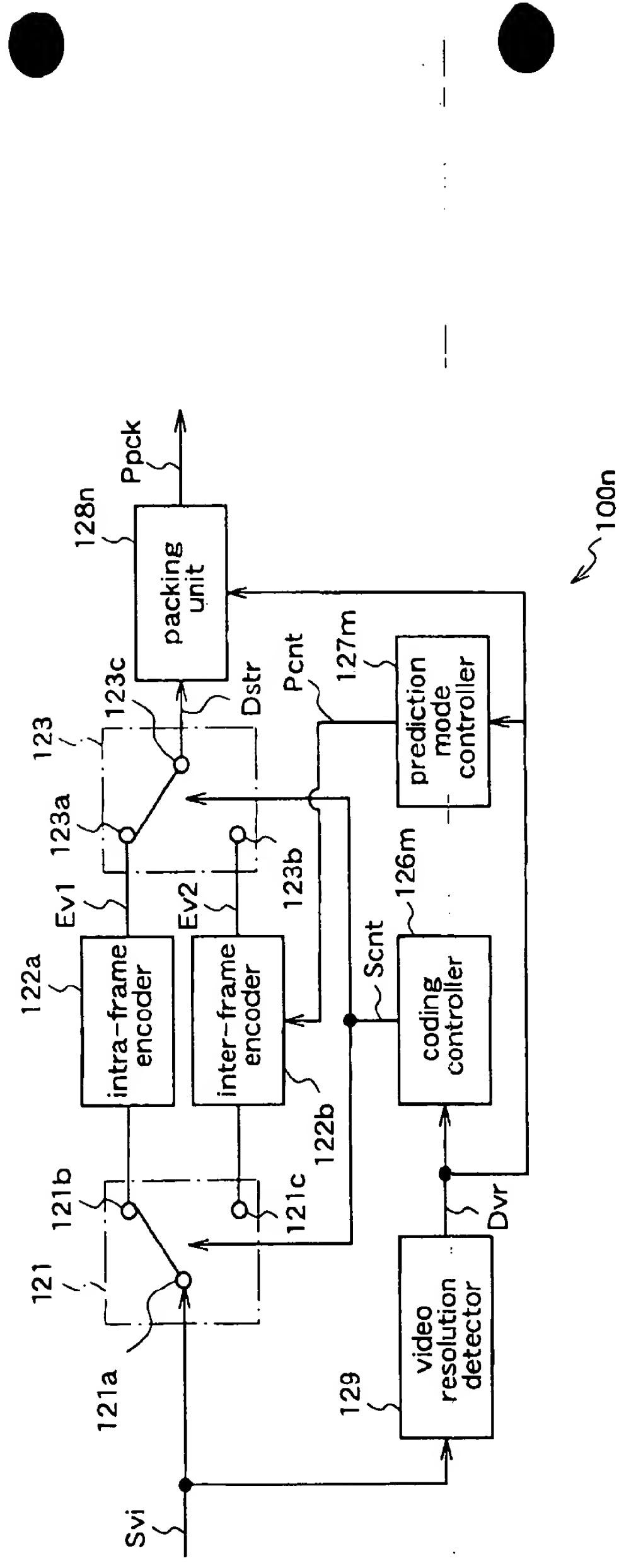
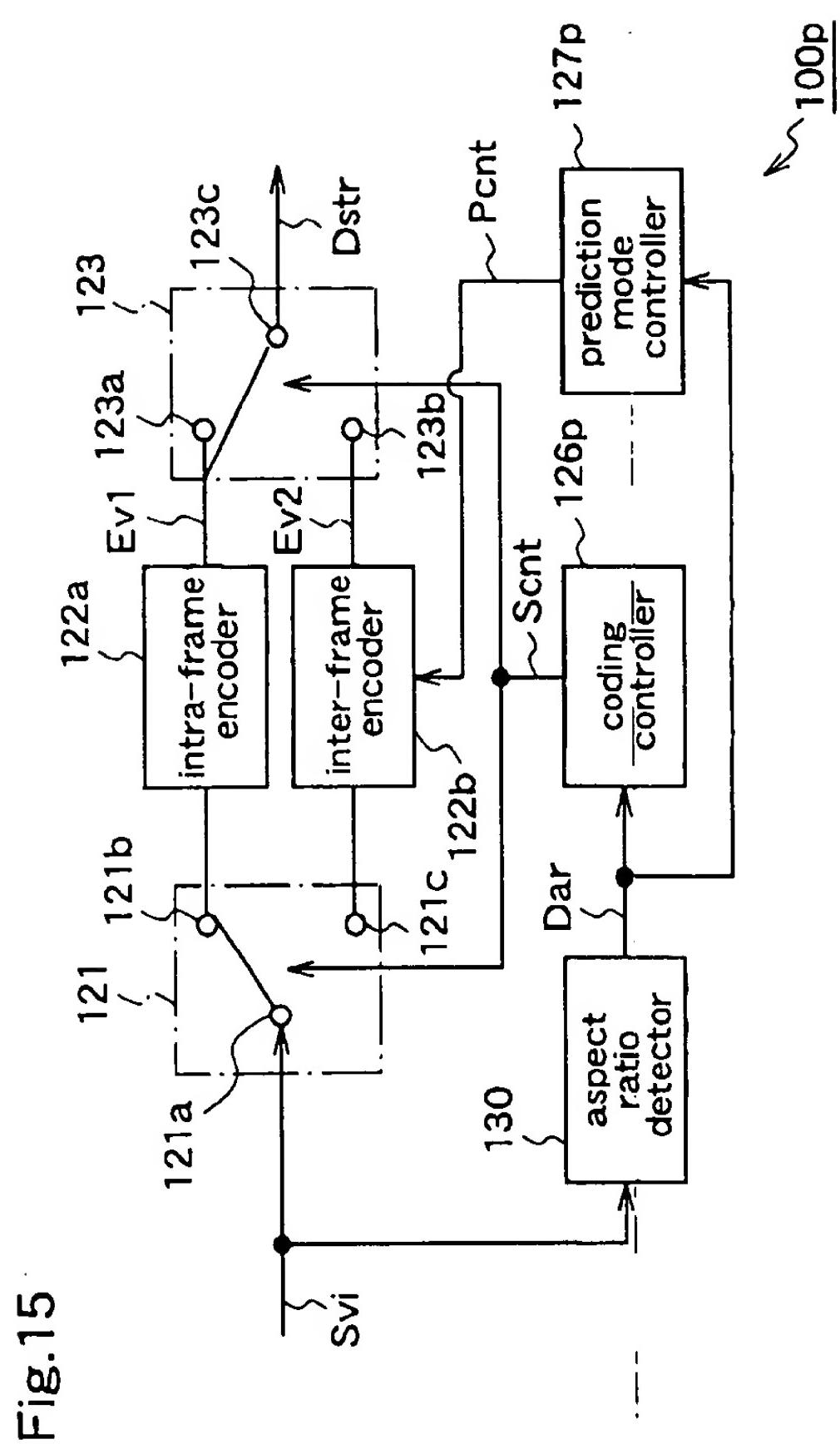


Fig. 15



121 122 123 124 125 126 127 128 129

Fig. 16

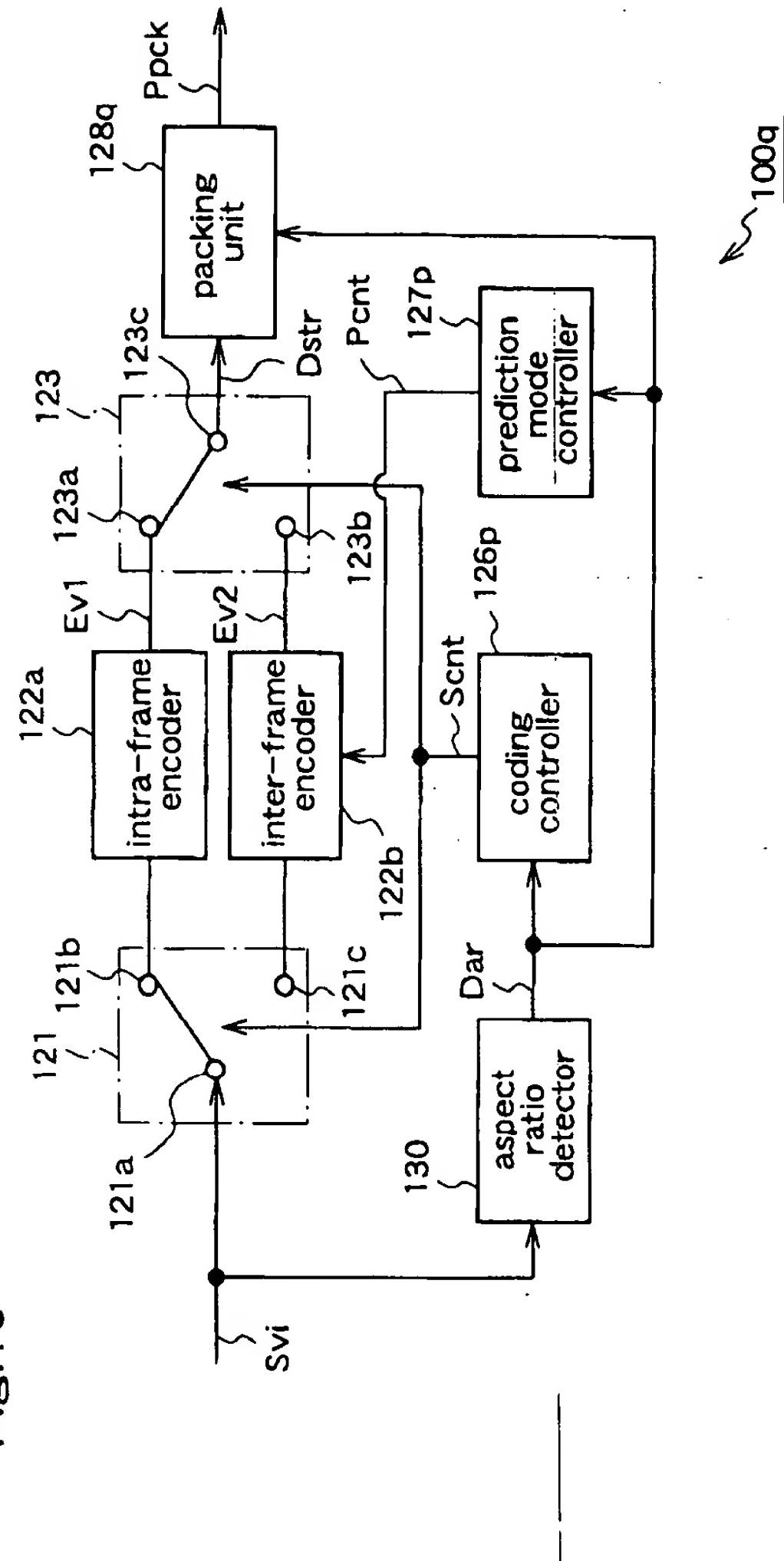
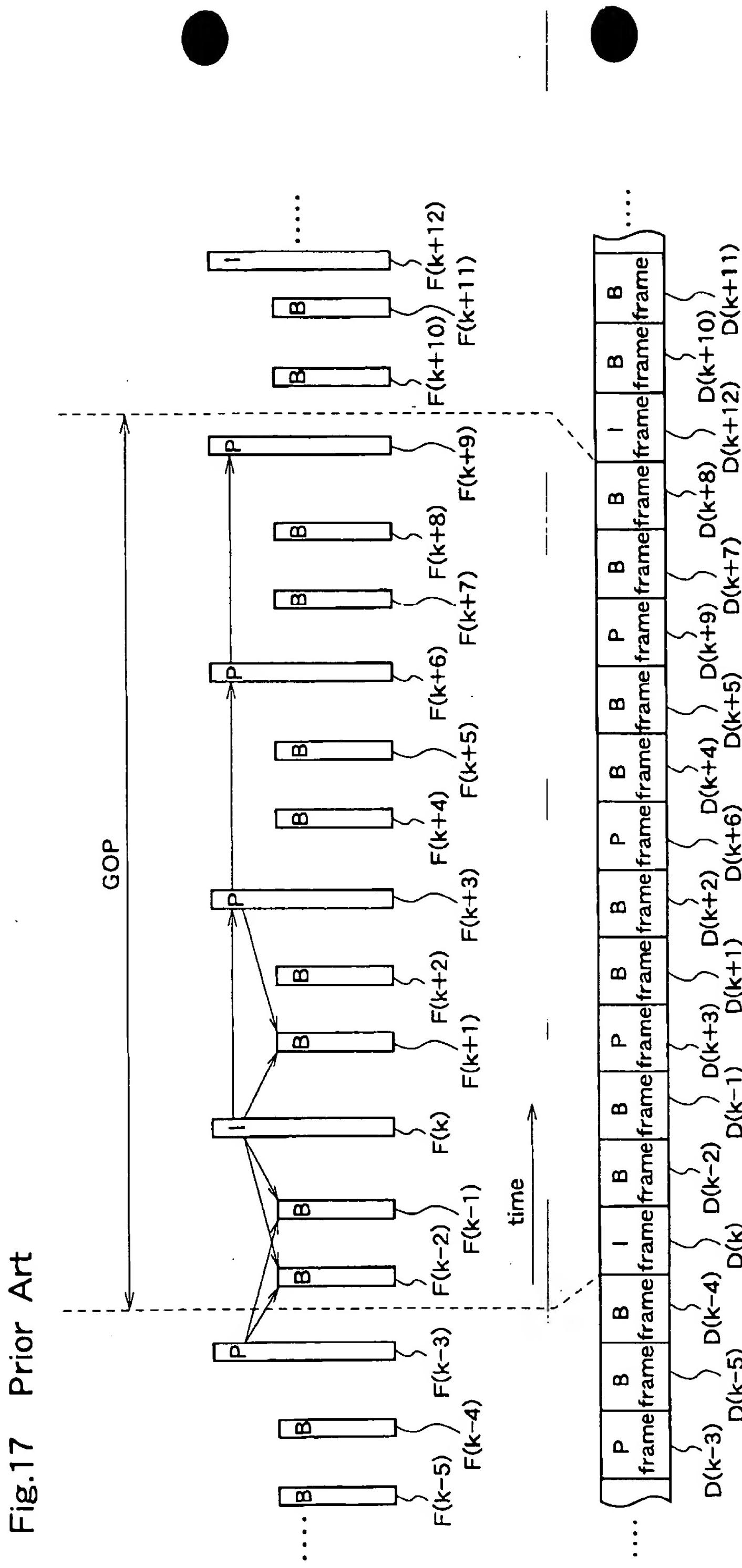
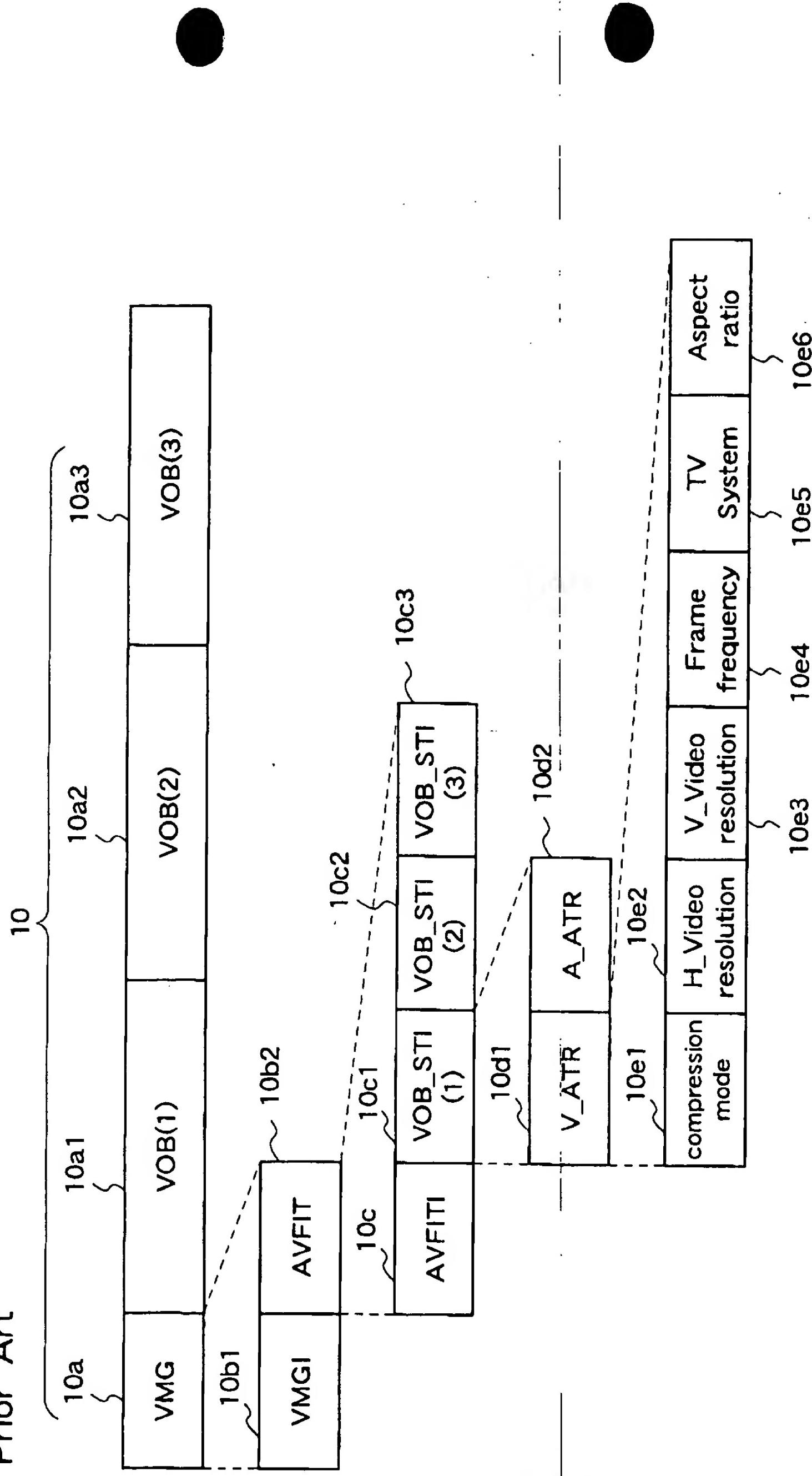


Fig. 17 Prior Art

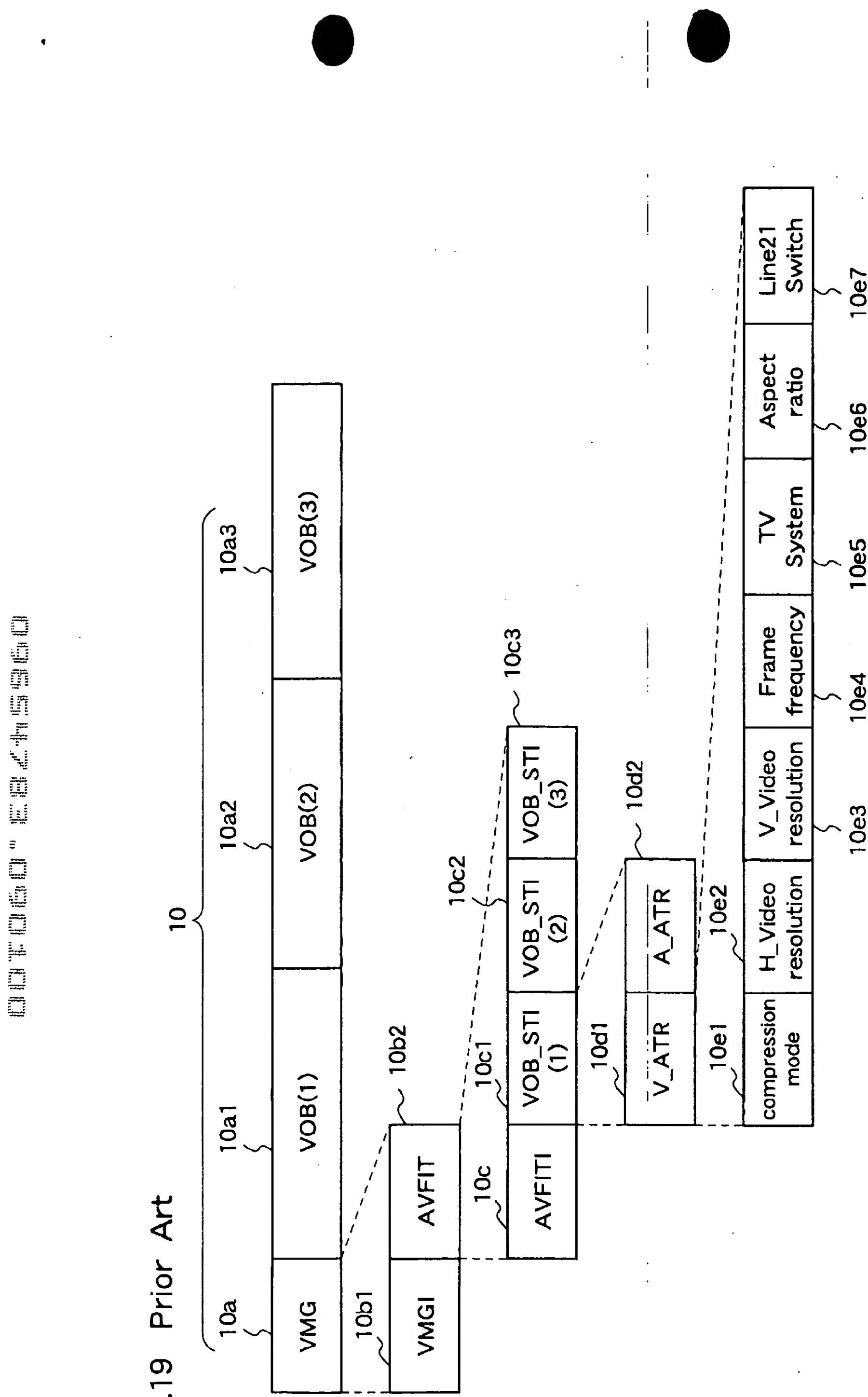


**Fig.18 Prior Art**

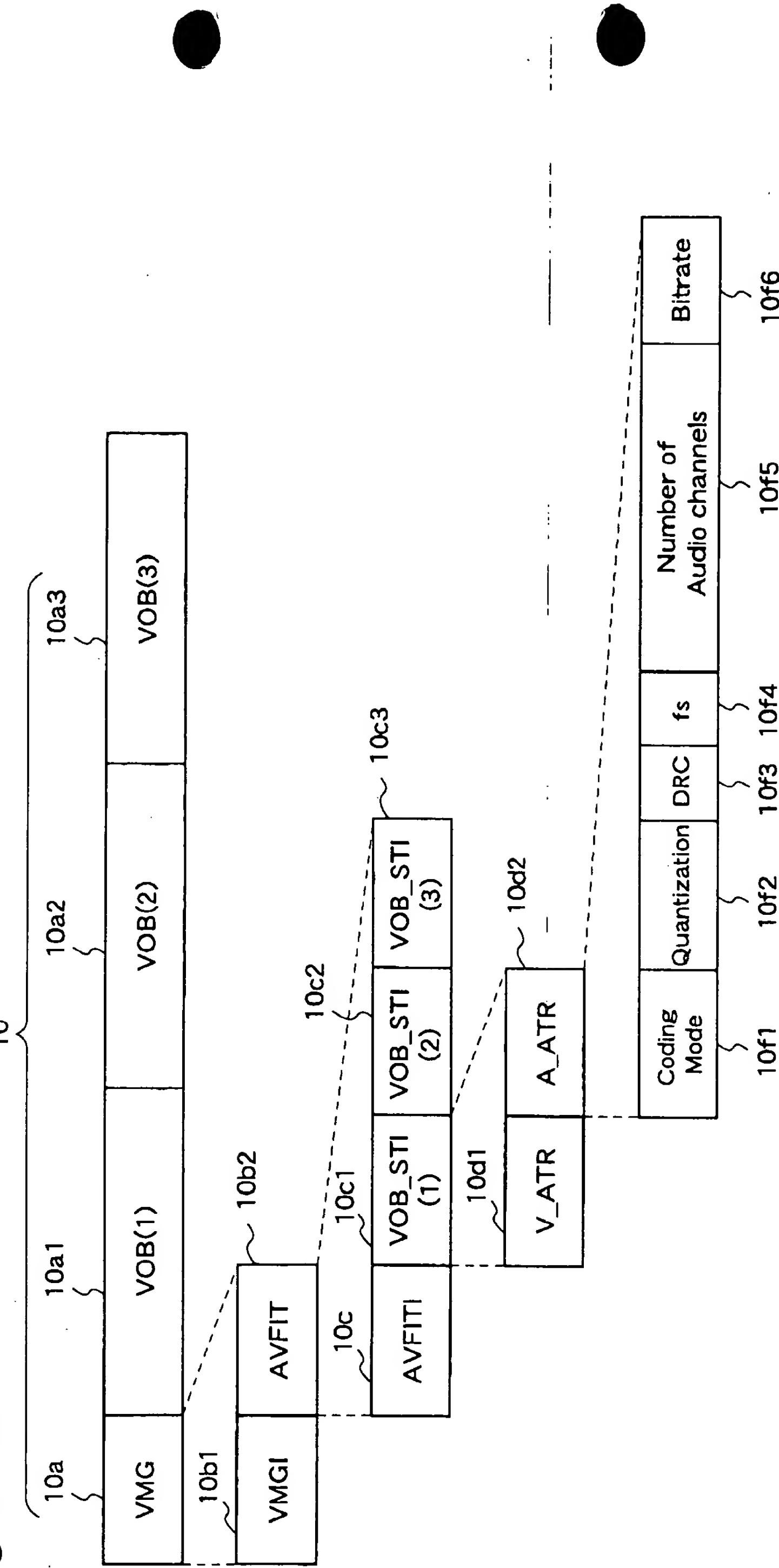
VMG VOB AVFITI V\_ATR A\_ATR



**Fig.19 Prior Art**



**Fig.20 Prior Art**



10

Prior Art

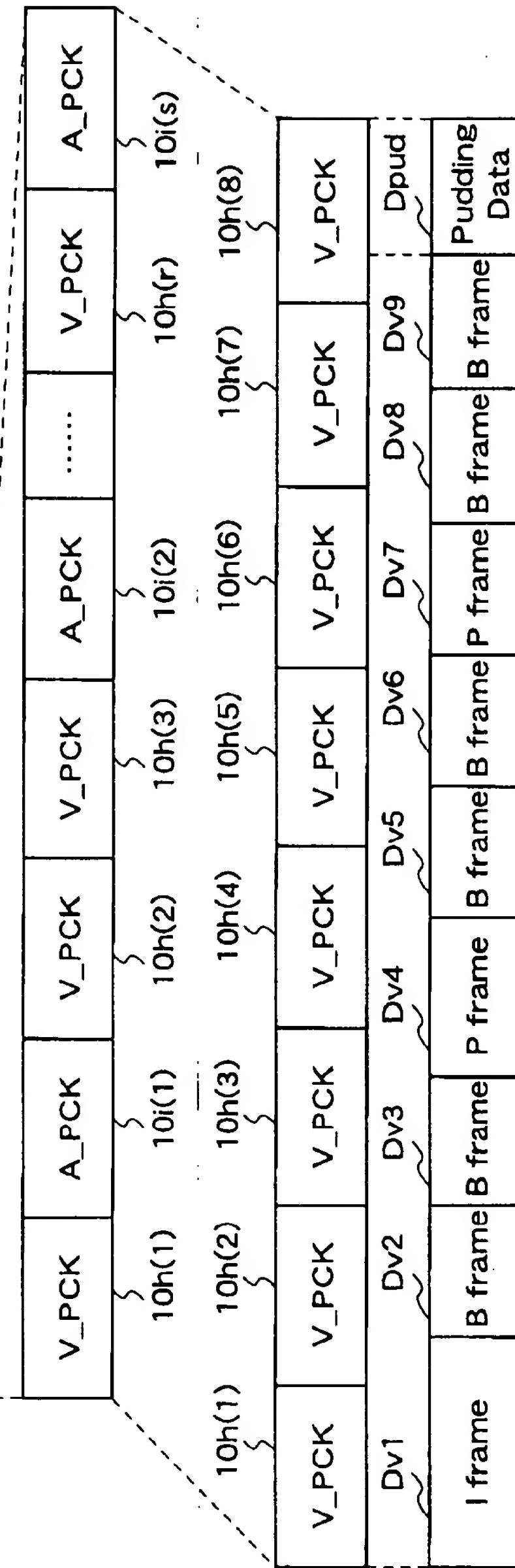
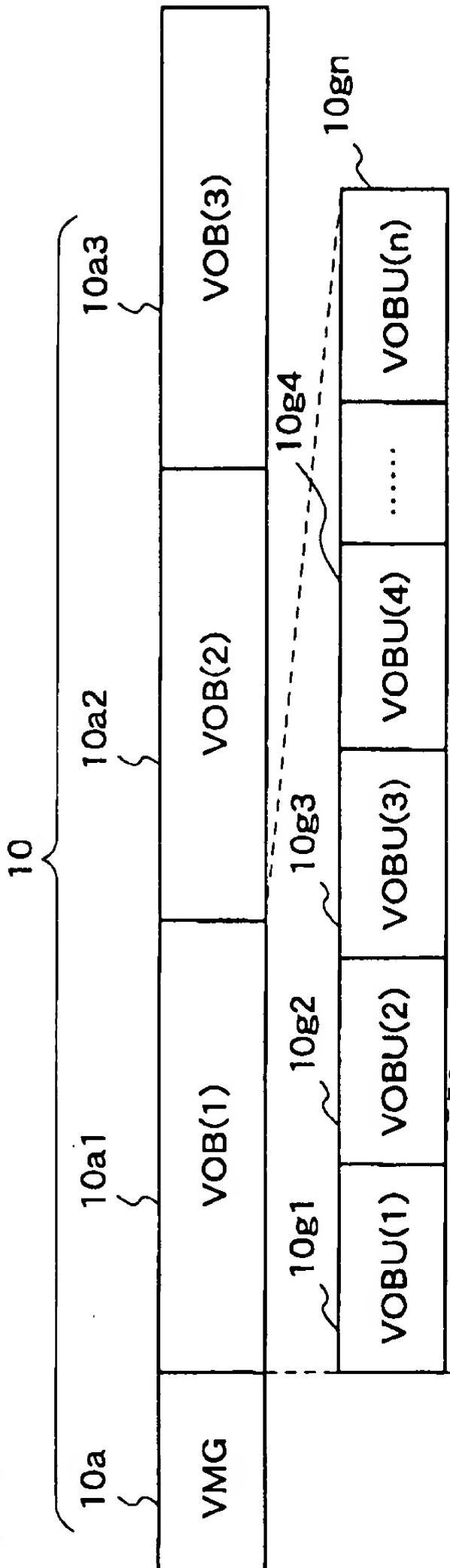




Fig.22 (a)

